

REMARKS

Claims 1-5 and 8 were pending and under consideration.

In the Final Office Action of May 30, 2003, claims 1-5 and 8 were rejected.

In response, claim 1 has been amended and claims 9 -11 have been added. Support for the new claims can be found on pages 11-12 of the specification. No new matter has been added.

The Examiner has rejected claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art in view of Jenq et al. (U.S. Patent No.: 6,153,465). The Examiner also has rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art in view of Jenq et al. and in view of Ghandhi. The Examiner has essentially alleged that cited references teach what is disclosed and claimed in the present invention. Applicants respectfully disagree and traverse this rejection.

Independent claim 1 recites a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film on a substrate and then growing spherical or hemispherical grains on the surface of the semiconductor film; diffusing an impurity to the grains grown on the surface of the semiconductor film; removing the impurity product, which is generated in the step of diffusing the impurity, from the surface of the semiconductor film using a non-etching cleaner selected from the group consisting of: 1) hot water, 2) a mixed solution of water, hydrochloric acid and hydrogen peroxide and 3) a mixed solution of sulfuric acid and hydrogen peroxide; and removing native oxide on the semiconductor film after the step of removing the impurity product. This is clearly unlike all of the cited references, which fail to disclose or even suggest a step to remove native oxide on the semiconductor film after removing the impurity by hot water.

In stark contrast, the admitted prior art specifically discloses forming a semiconductor film on a substrate growing polycrystallized grains on the surface, and then diffusing an impurity, but fails to disclose removing of impurity product, as the Examiner noted. While Jenq et al. discloses cleaning a semiconductor film using a solution containing hot water, it does not, however, disclose or teach that this step could be done with a non-etching cleaner. In fact, it specifically discloses use of an etchant in conjunction with hot water. (Jenq et al. Col. 1, lines 64-65). By using a non-etching cleaner, the defects between the bottom electrodes in the capacitor formed adjacent to each other are suppressed as much as possible and a capacitor with high reliability can be fabricated. (Spec. page 12).

Figure 8 of the present invention illustrates the difference between cleaning without etching and cleaning with etching. In the case where cleaning was done with a non-etching cleaner, such as hot water (which is used in the present invention), the number of defects generated between the adjacent bottom electrodes is substantially less than where cleaning was done with a etching cleaner, such as a mixed solution of NH_4OH and H_2O_2 (which is the same etchant used in Jenq et al.). (Col. 1, lines 64-65). Thus, unlike Applicants' claim 1, the cited references fail to disclose or fairly suggest a step of removing native oxide on the semiconductor film after the step of removing the impurity product using a non-etching cleaner selected from the group consisting of: hot water, a mixed solution of water, hydrochloric acid and hydrogen peroxide and a mixed solution of sulfuric acid and hydrogen peroxide.

Accordingly, it would not have been obvious to one skilled in the art at the time when the invention was made to combine the references as suggested by the Examiner to derive what is recited in claim 1.

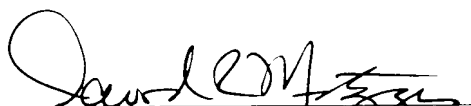
Claims 2-5 and 8 all depend directly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit these rejections have been overcome and request that they be withdrawn.

In view of the foregoing, it is submitted that the pending claims 1-5 and 8-11 are patentable and that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

SONNENSCHN NATH & ROSENTHAL LLP

 (Reg. No. 32,919)

David R. Metzger

SONNENSCHN NATH & ROSENTHAL LLP

Customer Account No. 26263

P.O. Box 061080 - Wacker Drive Station

Chicago, Illinois 60606

Telephone (312) 876-2578

Attorneys for Applicants

SONNENSCHN NATH & ROSENTHAL LLP

P.O. Box #061080

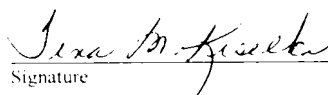
Wacker Drive Station-Sears Tower

Chicago, Illinois 60606-1080

(312)876-2578

MQT 11614285v2

I hereby certify that this document and any being referred to as attached or enclosed is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Commissioner for Patents, Mail Stop AF No Fee, P.O. Box 1450, Alexandria, VA 22313-1450, on **September 2, 2003**


Signature